

Tiago Carneiro Pessoa

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HPC Software Engineer and Researcher with extensive experience in performance analysis, benchmarking, and optimization of applications on large-scale distributed and heterogeneous systems. Strong background in MPI, OpenMP, and GPU programming, with hands-on experience supporting users and projects in deploying, scaling, and optimizing compute-intensive workloads on HPC platforms.

SKILLS

HPC & Programming	C/C++, Python, Chapel, OpenMP, CUDA, MPI, SIMD (SSE, AVX)
Performance Profiling & Analysis	NVIDIA Nsight Systems, NVProf, PERF, Intel VTune, LIKWID
Platforms & Tools: Linux/Unix	Git, Build Systems (CMake, Make), Containers (Docker, Singularity)
Domain Expertise	HPC, distributed systems, GPU computing, combinatorial optimization

LANGUAGES

- Portuguese (Native), English (full professional proficiency), French (professional working proficiency).

EDUCATION

PhD in Computer Science Federal University of Ceará (UFC). Fortaleza - CE, Brazil	2013 - 2017
Master's Degree in Computer Science State University of Ceará (UECE). Fortaleza - CE, Brazil	2010 - 2012
Bachelor's Degree in Computer Science State University of Ceará (UECE). Fortaleza - CE, Brazil	2004 - 2009

AWARDS AND HONORS

Outstanding Paper Award The International Conference on High Performance Computing & Simulation - HPCS 2020	Awarded 2021
Certification of Outstanding Contribution in Reviewing Journal of Parallel and Distributed Computing (JPDC)	2016

WORK EXPERIENCE - FROM PHD

Researcher Imec - Leuven, Belgium	Sep 2022 - Jan 2025
· Contributed to the design and development of a distributed PGAS-like programming library for novel HPC/AI platforms, together with associated profiling and benchmarking tools. · Designed and implemented a robust Bash-based distributed process management system to deploy, run, and analyze applications across HPC clusters, supporting performance studies and user workflows. · Implemented and analyzed representative HPC benchmarks (e.g., FEM, BLAS, HPCG) to study application scalability and performance behavior to validate system and hardware design choices.	

Research associate | University of Luxembourg - Belval, Luxembourg Mar 2021 - Sep 2022

- Designed and implemented large-scale distributed optimization algorithms for CPU–GPU heterogeneous systems, focusing on scalability, productivity, and parallel efficiency.
- Organized workshops and developed hands-on tutorial material on HPC topics for students and researchers.

Postdoctoral researcher | INRIA Lille - Nord Europe - Lille, France Nov 2018 - Jun 2020

- Co-created the Chapel-based Optimization Project (ChOP), a recognized initiative contributing to high-performance, distributed Branch-and-Bound algorithms.
- Designed and implemented large-scale distributed applications, balancing productivity and parallel efficiency using high-productivity languages (Chapel, Julia, Python/Numba) and HPC technologies (C/C++, OpenMP, MPI).
- Authored multiple papers in top-tier journals and conferences; taught Master’s courses and organized workshops on HPC and optimization.

Postdoctoral researcher | IFCE - Fortaleza, Brazil Mar 2018 - Oct 2018

- Supported the parallelization of deep learning for computer vision applications using Python multiprocessing.
- Used CUDA, OpenCV, and cloud-based platforms for GPU-accelerated experimentation and performance evaluation.
- Developed tutorial material on Python multiprocessing and contributed to strengthening parallel computing practices within the lab.

Doctoral Researcher | Federal University of Ceará - Fortaleza, Brazil Mar 2013 - Dec 2017

- Designed and implemented exact parallel and heterogeneous algorithms for combinatorial optimization.
- Achieved significant performance improvements by exploiting GPU acceleration with CUDA Dynamic Parallelism (CDP) and CPU parallelism using SIMD (SEE, AVX), MPI and OpenMP.

Visiting Researcher | INRIA Lille - Nord Europe - Lille, France Sep 2015 - Aug 2016

- As part of my PhD, I researched on parallel optimization algorithms with the Dolphin team, collaborating in an international research environment at INRIA Lille.

SELECTED PUBLICATIONS:

[1] Carneiro, T.; Melab, N.; Hayashi, A.; Sarkar, V. Towards Chapel-based Exascale Tree Search Algorithms: dealing with multiple GPU accelerators. In: The International Conference on High Performance Computing & Simulation - HPCS 2020 - held in March 2021. **Outstanding Paper Award - HPCS 2020.**

[2] Carneiro, T.; Kayraklioglu, E.; Helbecque, G.; Melab, N. Investigating Portability in Chapel for Tree-based Optimization on GPU-powered Clusters. The 30th International European Conference on Parallel and Distributed Computing - Europar 2024.  10.1007/978-3-031-69583-4_27.

[3] Carneiro, T.; Gmys, J.; Melab, N.; Tuytens, D. Towards Ultra-scale Branch-and-Bound Using a High-productivity Language. Future Generation Computer Systems, 105: 196-209 (2020).  10.1016/J.future.2019.11.011.

More information about my publication record and citations can be found in my  Google Scholar,  Orcid (0000-0002-6145-8352) and  Web Of Science (J-3061-2019) profiles.